Remarks

Claims 1-5, 10-15 and 18-23 are pending in the application. Claims 6-9, 16 and 17 have been canceled without prejudice or disclaimer. Claims 18-23 are newly added. Claims 1-5 and 10-15 stand rejected.

Claim rejections

Section 112

Claims 1-9 and 13-15 were rejected under 35 USC 112, 2nd paragraph. Of these claims, claim 1-5 and 13-15 remain pending.

In the section 112 rejection, the Examiner alleges that it is unclear "who perform[s] the 'obtaining exclusive access' step" and that it is unclear "who perform[s] 'querying'." The Examiner further indicates that "it is not clearly understood what happen[s] after resource descriptor reserve resources for exclusive use by the first logical processor (i.e. waiting or release)" and that it is "unclear when and how the 'the releasing' step is perform[ed] and who perform[s] this step."

The Applicant respectfully reiterates that the rejected claims comply fully with 35 USC 112, 2nd paragraph, which only requires that claims "particularly point[ ] out and distinctly claim[ ] the subject matter which the applicant regards as his invention." The rejected claims do so.

For example, claim 1 recites "obtaining exclusive access for a first logical processor to a resource descriptor describing a usage allocation of said shared resources." It is immaterial to particularity or distinctness "who performs" this operation. As regarded by the Applicant, the invention comprises the operation as stated; the Applicant does not regard the invention as being defined by what entity or agent performs the operation.

This is within the Applicant's sphere of discretion. It is respectfully submitted that the Examiner is improperly encroaching on this sphere by reading a non-existent requirement into 35 USC 112, 2nd paragraph: the requirement to state "who performs" an operation of a method. The patent database is replete with claims that, just as the presently rejected claims, are devoid of any limitations as to "who performs" operations of a method. This signifies the universal recognition that there is no requirement for any

such limitation. Withdrawal of the rejection of claims 1-9 and 13-15 under 35 USC 112, 2nd paragraph is therefore respectfully requested.

Section 103

Claims 1-3 were rejected under 35 USC 103(a) as being unpatentable over Hays, Jr. et al. (US Patent No. 4,354,227) ("Hays").

The Applicant respectfully submits that the asserted rejection cannot be sustained for at least the reason that Hays does not suggest "obtaining exclusive access for a first logical processor to a resource descriptor describing a usage allocation of said shared resources" as claimed.

In the Advisory Action, the Examiner cites col. 10, lines 18-19 and col. 8, lines 24-26 of Hays as disclosing the noted feature. The Examiner states that "Hays teaches the current contents of control register for shared resource ... and the condition cod[e] is [s]et to indicate that the given processor has sole control of the resource."

It is not disputed that Hays discloses reserving resources via a control register. However, Hays lacks the multiple levels of control provided by the present invention as claimed. The present claims require both a resource descriptor to reserve resources, *and* an added level of control: a semaphore register to reserve access to the resource descriptor. That is, a logical processor cannot obtain access to the resource descriptor unless granted access by the semaphore register. This way, it can be guaranteed that the contents of the resources descriptor do not change while a particular logical processor tries to reserve resources.

Hays simply does not disclose this added level of control. Hays only has a single level of control -- i.e., only directly at the resource level.Hays does not disclose any way to reserve the control register that is used to reserve resources. In fact, to the contrary, Hays' method is used *because* the control register cannot be reserved; again, col. 2, lines 9-12 explicitly say that "*no* processor can be granted sole access to a common storage location utilized for controlling access to the common shared resource ..." (emphasis added). Hays further explicitly describes how one processor can overwrite another processor's reservation of a resource, and proposes a "wait cycle" to

"determine which processor is actually authorized to take control of the resource." See Hays, col. 2, lines 36-43. Accordingly, claim 1 is allowable over Hays. Claims 2 and 3 are likewise allowable over Hays, for at least the reason that they include the features of claim 1 by dependency thereon. Withdrawal of the rejection of claims 1-3 as unpatentable over Hays is therefore respectfully requested.

Claims 4 and 5 were rejected under 35 USC 103(a) as being unpatentable over Hays in view of Scalzi (US 5,895,492).

Claims 4 and 5 include the recitations of claim 1 by dependency thereon. Hays is silent as to claim 1's "obtaining exclusive access for a first logical processor to a resource descriptor describing a usage allocation of said shared resources" as discussed above. Scalzi does not remedy the deficiency in Hays. Scalzi relates a method of data recovery when a processor using a shared resource fails, but in no way suggests the noted feature of claim 1. Accordingly, claims 4 and 5 are allowable over Hays and Scalzi for at least the reason that they include this feature. Withdrawal of the rejection of claims 4 and 5 as being unpatentable over Hays and Scalzi is therefore respectfully requested.

Claims 6-12 and 16 were rejected under 35 USC 103(a) as being unpatentable over Hays in view of DeKoning et al. (US 6,823,472) ("DeKoning"). Of claims 6-12 and 16, claims 10-12 and 16 remain pending. The Applicant respectfully traverses the rejection of claims 10-12 and 16.

As to independent claims 10 and 16, these claims are allowable over Hays and DeKoning for at least the reason that neither reference suggests a semaphore to reserve exclusive access for one of a plurality of logical processors to a resource descriptor as recited. The Examiner cites Hays at col. 2, lines 8-12 and col. 10, lines 16-19. However, these passages do not suggest the noted feature. Instead, as discussed earlier in connection with claim 1, col. lines 8-12 of Hays actually say the opposite: " ... no processor can be granted sole access to a common storage location utilized for controlling access to the common shared resource ...". DeKoning is also silent as to reserving sole access to a resource descriptor. Accordingly, claims 10 and

16 allowable over Hays and DeKoning. Claims 11 and 12 are likewise allowable over Hays and DeKoning for at least the reason that they include the features of claim 10 by dependency thereon.

In view of the foregoing, withdrawal of the rejection of claims 10-12 and 16 as unpatentable over Hays and DeKoning is respectfully requested.

Claims 13-15 were rejected under 35 USC 103(a) as being unpatentable over Hays in view of Florek (US 6,795,901).

The Applicant respectfully traverses. Claims 13-15 are allowable over Hays and Florek for at least the reason that neither references suggests "setting a lock bit in a semaphore register to reserve exclusive access to a resource descriptor register" as recited in independent claim 13. This has been amply demonstrated with respect to Hays in the preceding discussion.

Florek does not cure the deficiencies in Hays. The portion of Florek cited by the Examiner, col. 10, lines 39-42, does not relate to reserving exclusive access to a resource descriptor, but to a resource itself.

The Examiner contends in the "Response to Arguments" section of the Office Action that "Florek clearly teaches modifying the mutex takes the form of an increment operation in which a processor raises the value of the flag (lock bit) variable to signify concurrent possession of the resource," citing Florek at col. 10, lines 39-42 (Office Action, page 13, item 40(C)). Along lines discussed previously, the Applicant respectfully submits that this is not material to patentability because what the Examiner points out in Florek is not what is claimed. The claims recite reserving exclusive access to a resource descriptor; Florek contains no such disclosure. Accordingly, claim 13 and claims 14 and 15 dependent thereon are allowable over Hays and Florek. Withdrawal of the rejection of claims 13-15 as being unpatentable over Hays and Florek is therefore respectfully requested.

Claim 17 was rejected as being unpatentable over Hays, DeKoning and Scalzi. Claim 17 depends on claim 16. Claim 16 is allowable over Hays, DeKoning and Scalzi for at least the reason that it recites a semaphore to reserve exclusive access for one of

a plurality of logical processors to a resource descriptor. None of Hays, DeKoning or Scalzi suggests this feature, as demonstrated in the preceding discussion. Withdrawal of the rejection of claim 17 as unpatentable over Hays, DeKoning and Scalzi is therefore respectfully requested.

New claims

New claims 18-23 allowable over the art of record for at least the reason that, along lines discussed above, the art of record does not suggest "access control logic to allocate one or more of said shared resources only when granted exclusive access to said resource descriptor by said semaphore register," as claimed.
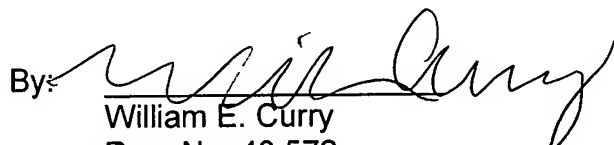
Conclusion

In light of the above discussion, Applicant respectfully submits that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

Dated: JAN. 10, 2006

By: _____
William E. Curry
Reg. No. 43,572

KENYON & KENYON
1500 K Street, N.W., Suite 700
Washington, D.C. 20005
Tel: (202) 220-4200
Fax:(202) 220-4201